

Fig. 1
(PRIOR ART)

Address		
Bus	Node	Initial Memory Space

Fig. 2
(PRIOR ART)

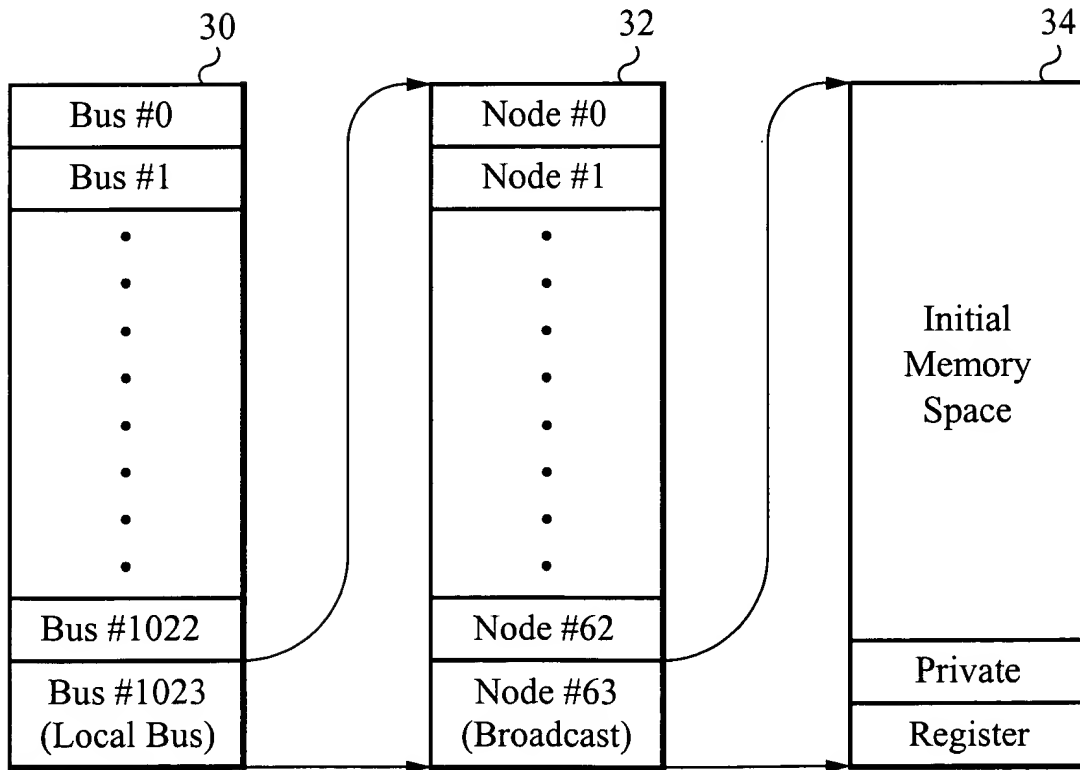
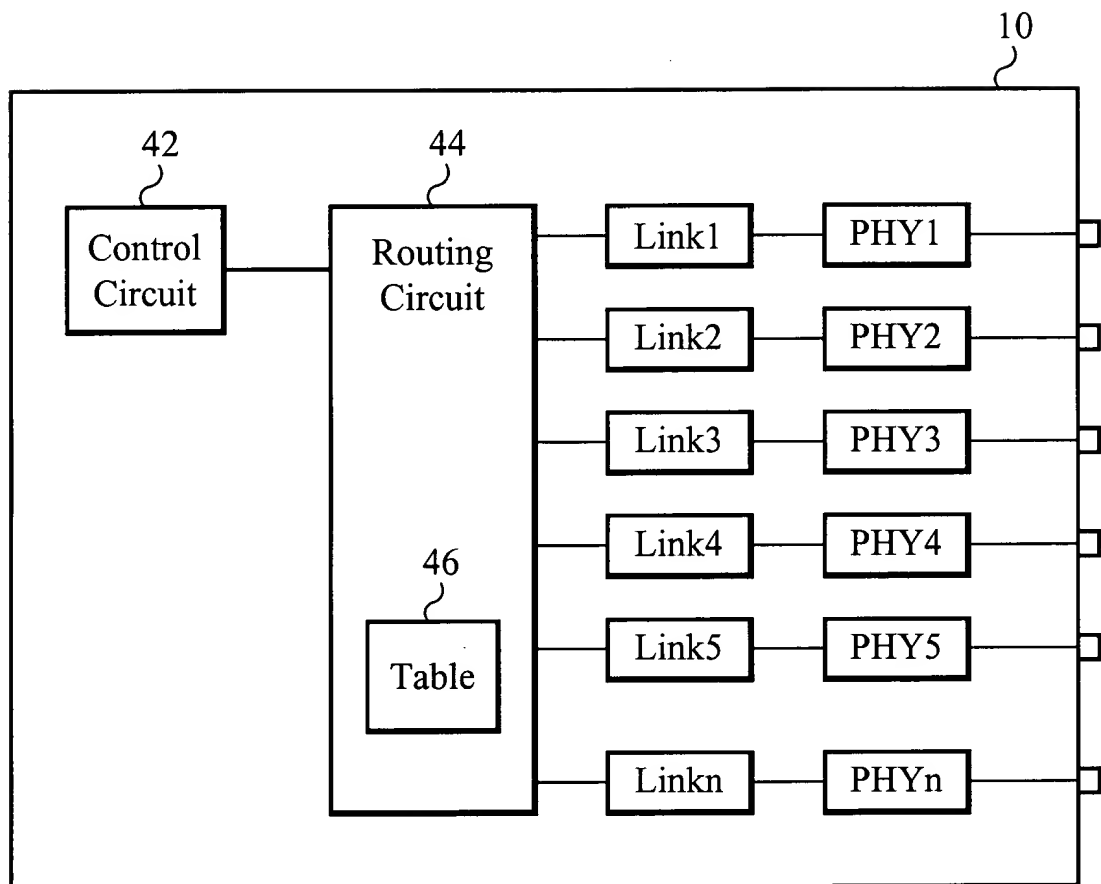
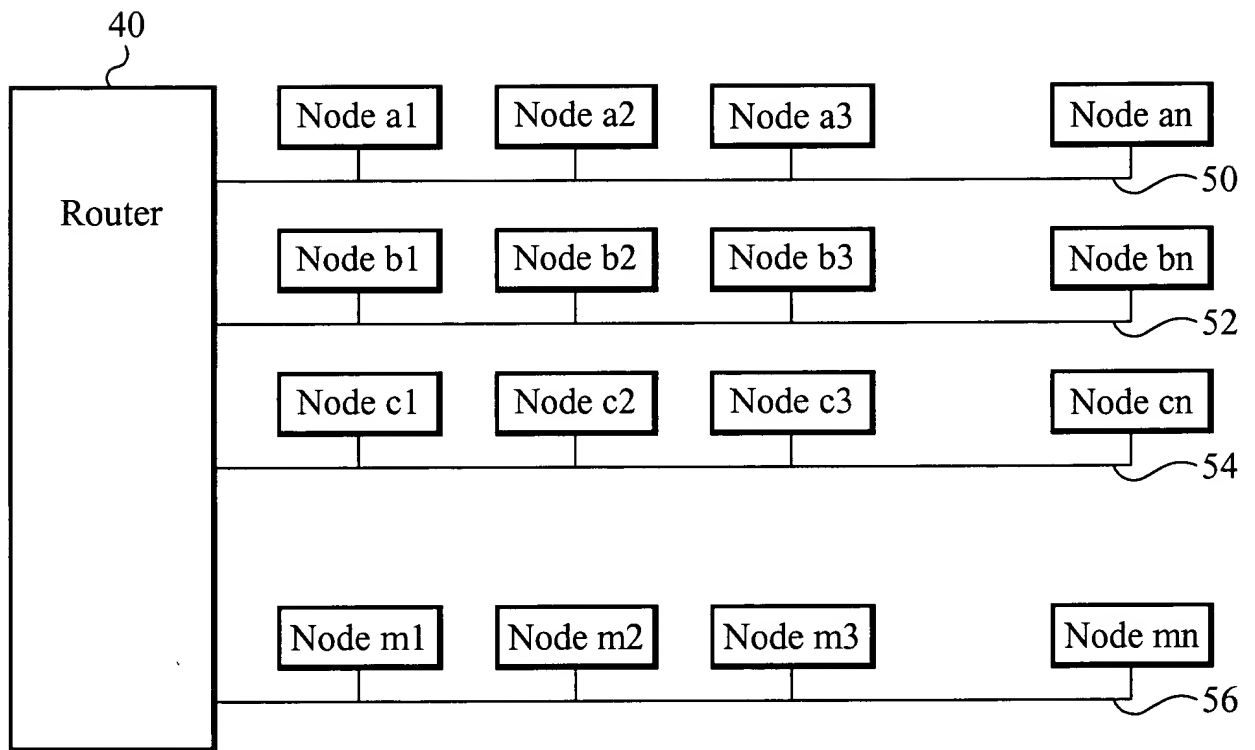


Fig. 3
(PRIOR ART)

**Fig. 4**

**Fig. 5**

Bus	Node	Tag	Bus#	Node#	Offset Value
10	6	2	4	6	36

Fig. 6

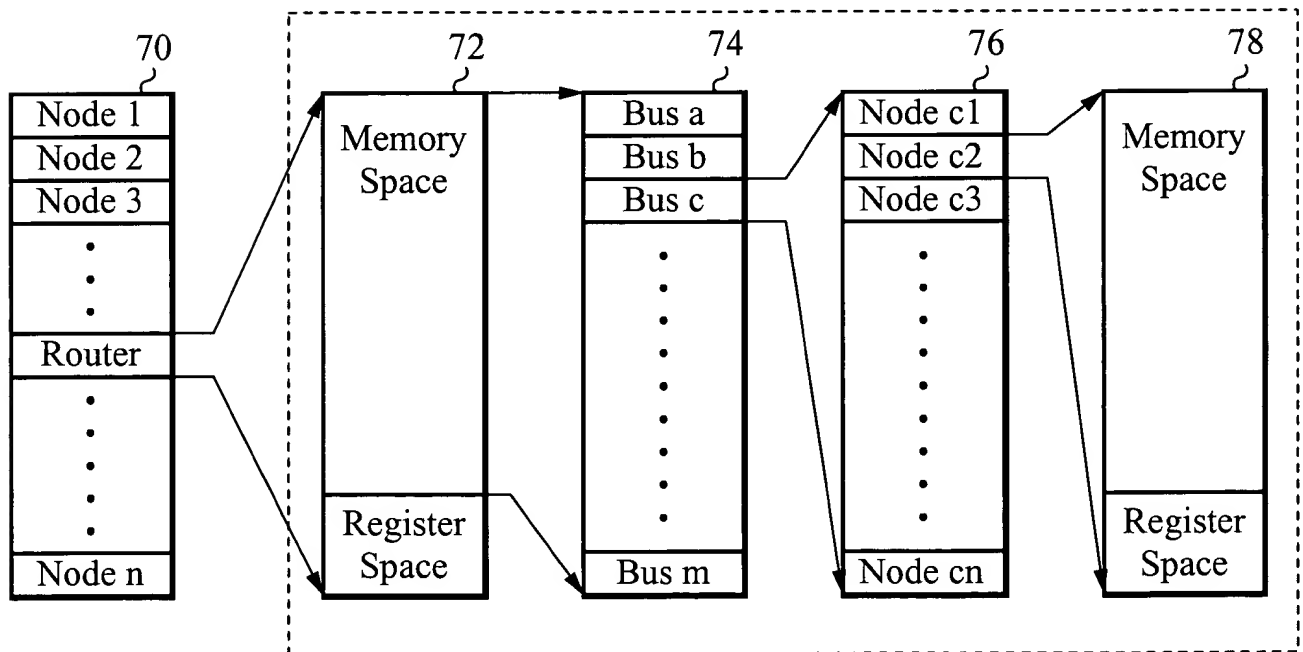
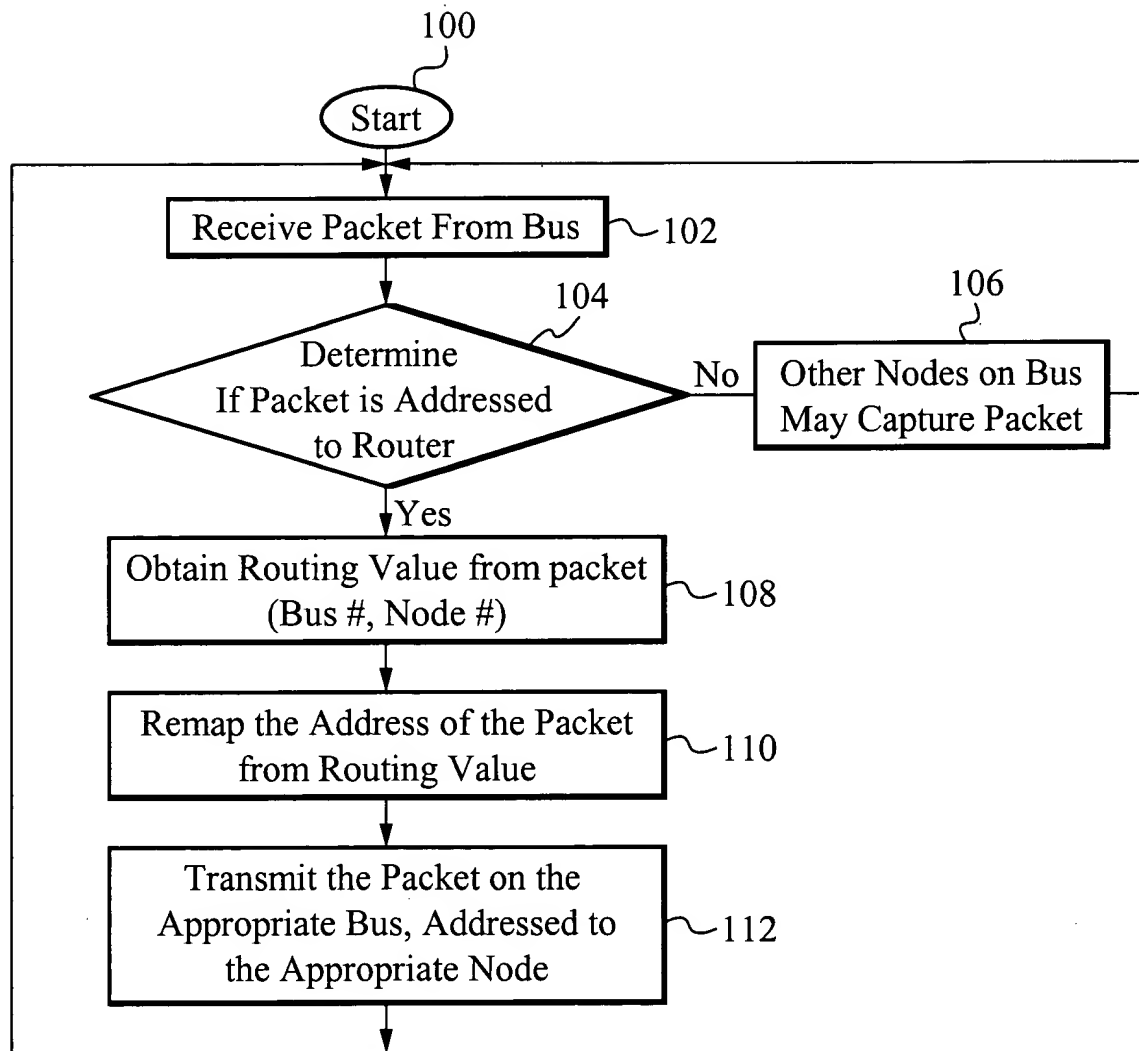
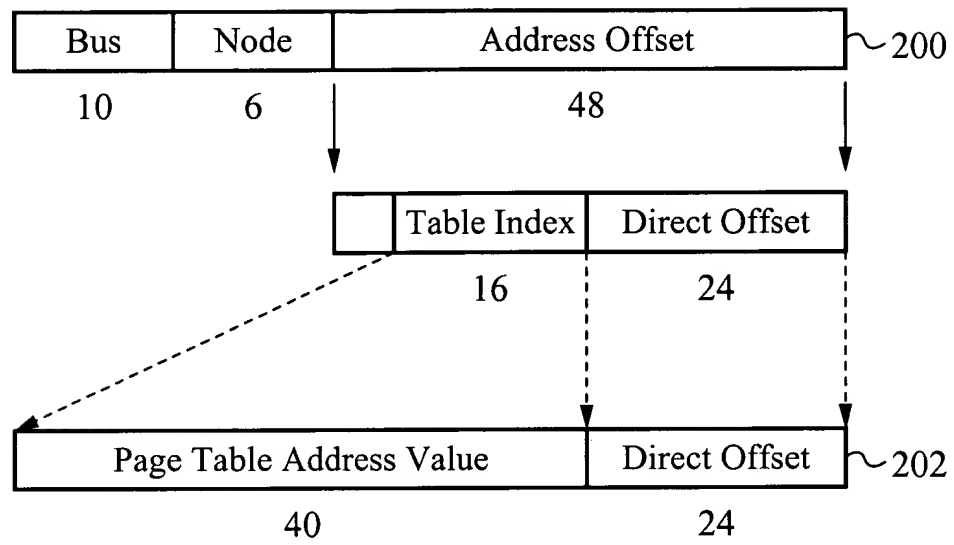


Fig. 7

**Fig. 8**

**Fig. 9**